REMARKS

Claims pending in the application are 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54, 56-74 and 76-85.

Claims 2, 4, 7, 9, 11-14, 17, 21, 27, 29, 35, 37, 39-44, 51, and 55 and 75 have previously been canceled in this case.

PRIORITY

Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is no longer needed. These required references are all in the continuation-in-parts parent applications file wrappers, and have previously already repeatedly cited. The examiner would have seen them in the file wrappers.

A "Family Tree" Exhibit A on Li's atomic IC inventions and a new Exhibit B on IC features sizes (Moore's Law) are submitted herewith to replace the applicant-cited references in the 23 Nov. 2007 amendment . These Exhibits also answer the new final rejections based Li's '800 patent. They further particularly point out and distinctly claim this invention.

The examiner withdrew the nonstarter double patenting rejections of claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 52-54 and 56-85, and other rejections, without citing any of these cited references. This suggests that these previously cited references are not useful any more.

Claim Objections

Claims 3, 15, 19, 20, 38, 47, 49, 50, 56, 58, 63, 73, 78, 79, 80 and 85 are objected to because of informalities. Appropriate corrections have been made to remove informalities and to make these claims allowable.

Claim Rejections - 35 U.S.C. 112, first paragraph

The arguments and other evidences presented herein overcome all the new final rejections of all the claims. Further, all these new evidences are necessary and were not earlier presented because of examiner's new final rejections dated February 7, 2008.

Claims 3, 19, 23, 38 and 60 are rejected under 35 U.S.C. 112 first paragraph, as failing to comply with the written description requirement. Claims 56 and 71 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

After appropriate amendment, these claims now contain subject matter which was described in the specification in such a way as to reasonable convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Specifically, in claims 3 and 23, dimension limitations, such as vertical thickness of less than a few hundred atomic layers, are replaced by dimensional accuracy of or better than a few hundred atomic layers, as suggested by the examiner.

selected top major surface and a selected bottom major surface ~~surfaces~~ of said solid material pocket, a selected top major surface and a selected bottom major surface ~~surfaces~~ of said rectifying barrier, and a selected top major surface ~~surfaces~~ and a selected bottom major surface ~~surfaces~~ of said solid state material region are non-parallel to a number of said other selected surfaces;

said number being selected from the group consisting of one, two, three, four, five, six, and seven; and

said selected surfaces being both vertically and laterally within one micron of each other or one another.

81. (Previously Presented) A commercially mass-produced IC of claim 1 in which said solid substrate has a first top major surface and a second bottom major surface, and said electronic rectifying barrier has a third top major surface and a fourth bottom major surface;

at least one of said first, second, third, and fourth major surfaces being non-parallel to at least a number of said other three major surfaces;

said number being selected from the group consisting of one, two, and three;

at least selected portions of said first, second, third, and fourth major surfaces being all within two microns of each other or one another.

82. (Previously Presented) A commercially mass-produced IC of claim 1 in which said rectifying barrier directly contacting said solid state material region has one of the following shapes: a) at least a selected portion of the contacting rectifying barrier is non-flat; b) at least a selected portion of the contacting rectifying barrier is curved; c) at least a major portion of the contacting rectifying barrier is non-flat; d) at least a major portion of the contacting rectifying barrier is curved; e) said contacting rectifying

barrier is non-flat in its entity; f) said contacting rectifying barrier is curved in its entity; g) said contacting rectifying barrier is non-flat substantially in its entity; and h) said rectifying barrier is curved substantially in its entirety.

83. (Currently Amended) A commercially mass-produced IC of claim 1 in which, on a vertical cross-section thereof, selected respective portions of a top major surface of said solid substrate, a bottom major surface of said solid material pocket, and a top major surface of said rectifying barrier are all curved;

at least one of said three selected curved portions has a first peripheral surface contacting, at a contact area, a second peripheral surface of another of the three selected curved portions;

said first peripheral surface being differentially surface-expanded at said contact area over an area selected from the group consisting of: (a) a specified portion thereof; (b) a major portion thereof; (c) the entirety thereof; and (d) substantially the entirety thereof.

84. (Previously Presented) A commercially mass-produced, solid state, integrated circuit device of claim 57 in which said device material region comprises a cooling fluid.

85. (Currently Amended) ~~An~~ A commercially mass-produced IC of Claim 1, wherein said solid-state material region has a bottom located within a specified vertical distance from a selected point inside said rectifying barrier;

said specified vertical distance being selected from the group consisting of: a) one micron; b) 0.1 microns; c) substantially zero; d) between 0 and 0.1 microns; and e) between 0 and 0.1 microns but closer to 0 microns than to 0.1 microns.

In claims 19, 38, 58 and 60, "said solid state material region consists essentially of a solid material selected from the group consisting of oxide, glass, organics, semiconductor, non-semiconductor, intrinsic semiconductor, a solid comprising metal, intermetallics, dielectric material, and an electrically insulating solid". The materials such as oxide, glass, organics, non-semiconductor, intrinsic semiconductor, a solid comprising metal, intermetallics, dielectric material, and an electrically insulating solid are all non-semiconductors. Introducing metal or other foreign elements into groove is shown on, for example, page 31, lines 25-29. And page 32, lines 8-33, and page 33, lines 12-15.

In claims 52 and 65, limitations on aspect ratios have been deleted. Claims 56 and 71 have also been amended to have now sufficient antecedent bases in the claims to properly have the required cited limitations.

Claim Rejections - 35 U.S.C.102

Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 22-26, 28, 30-34, 36, 38, 45-50, 57-64, 72-74 and 76-85 are rejected under 35 U.S.C. 102(b) as being anticipated by Li (U.S. Patent #4946800).

New arguments and evidences (Exhibit's A and B) are presented herein to overcome all the new final rejections of all the claims based on Li's old patent '800. These new evidences require none of the above-mentioned cited references, which are too irrelevant and moot to be needed any more, particularly at this late stage of the after-final examination. All these new evidences are necessary and were not earlier presented because of examiner's new final rejection in February 2008.

Accordingly, applicant would like to replace, by the newly cited

Exhibits, the previously cited references submitted before, for the following reasons:

A. The '081 cited reference are too irrelevant and moot. They are no longer needed probably by the examiner and certainly by the applicant;

B. The '081 Li's devices are nano or atomic IC devices, no longer the old basic though improved MOS and CMOS IC devices of Li;

C. Of the two newly cied exhibits, one is basically the well-known, well-respected Moore's law everybody follows; and the other new exhibit is a never-presented, Family Tree of Li's atomic IC devices;

D. Unlike the previously cited references, both the new Exhibits are self-evident and very short. In comparison, the examiner-cited reference on the Toshiba-Li suit alone involves two sharply different judges in qualifications, patent knowledge, technical knowhow, decisions, length of the court durations. Boxes of documents are available. Now that USPTO is promoting electronic over paper documentations; and

E. These new exhibits minimize and simplify the cited references, particularly in pointing out and distinctly claiming the invention.

According to the electronic engineering times, Feb. 15, 1993, page 6, the device feature sizes were way over 10 microns, with much less than 1,000 transistors, diodes, or other components on each chip. Submicron devices were impossible because of lack of design, equipment, and processing procedures. See the attached feature size chart of Fig. 1. In 1973, nobody in the world could, and dared to, make CMOS smaller than one micron sizes.

The '800 and '081 disclosures are thus totally different in IC

technologies. Hundreds or thousand valid U.S. patents separate these wo applications. Even though both are on Li's CMOS process designs, but the equipment, procedures, characteristics, and the like are patentable widely different.

Notice also that the '081 claims only "commercially mass-produced integrated circuits that have high yields and low costs to withstand fierce worldwide, tough competition. Each '081 device chip has thousands or millions times more device components. Even with the same component yield factor of, for example, 95% or even 99%, the final product chip yield is commercially reasonable and profitable with the '800 process, but practically zero with the '081 process.

Hence, applicant respectfully submits that these rejections have been overcome, because the Li's '800 patent does not enabling teach. One need only the famous Moore's Law to prove this. This law has been religiously respected and used by all IC technologists including Nobel Prize winners, prestigious professors from honored universities, chief technical personal, and all other IC technologists. This law decisively shows that in 1973 when the '800 patent was filed, the IC feature sizes were orders of magnitude larger than those in January 2004 when the '081 was filed. Nobody in the entire world could, or even dare, to make, in 1973 IC devices, with feature sizes less than the Law indicated. It will be shown that to reduce the IC feature size by an even mere seemingly negligible 10% may require thousands of IC technicians all scattered around the world to work hard for several years, buying many billions of dollars of new equipment alone, and even inventing dozens or hundreds of new **patented** IC technologies.

Electronic Engineering Times, February 15, 1993, on page 6 publishes two (left figure a, and right figure b) charts on "Solid State Semiconductor Scaling Close to Its Limits." See Exhibit B. These charts are respected and religiously obeyed and followed,

worldwide, by all IC professors, technical managers, and technicians The charts show that by 2000, lithography allows fabrication (or commercial mass-production for profit) of 0.1 micron IC feature sizes and 1 billion-transistor IC. Economic and manufacturing considerations often caused the companies to be more conservative, and to produce "no more than 100 or 250 million transistors on a circuit by 2000."

The attached left IC chart (chart a) shows that in 50 years from 1960 to 2010, the gate oxide thickness of all IC decreases by four orders of magnitude from about 1 microns to about 0.0001 microns the size or thickness. The component (e.g., transistors) feature size also decreased during the same period by about four orders of magnitude. For 30 years from 1970 to 2000, each memory or logic IC chip increased the number of component transistors from about 1K to 0.2 G.

Hence, in 1973, the filing date of Li's '800 patent ('102 application), the gate thickness was about 0.6 microns, and feature size about 19 microns; while he number of transistors per chip is about 10K. In 2004, the filing date of Li's '081 application, the gate electrode thickness is about 0.003 microns, while he feature size is about 0.1 micron.

There were no IC technologies and manufacturing equipment in 1973 to commercially mass-produce (at good yield and profit) Li's '081 miniaturized IC devices with "microscopic" feature sizes, dimensions, accuracies, precisions of **a few microns**. See '800 at column 11, lines 26-32.

Accordingly, the Li's '800 patent could not disclose any relevant and enabling IC designs and production technologies for commercially mass-producing, at good profit, the '081 devices. There were simply

none. The '081 devices were, in 2004, **orders of magnitude** smaller in feature sizes, critical gate layer thicknesses, and packing densities than what were possible or patented, by Li or anybody else.

It is well known that small differences in sizes, dimensions, and accuracy are not patentable. Do the **orders of magnitude** size differences between the '800 and '081 inventions patentable? These is no absolute numbers to distinguish between patentability and non-patentability. Other factors must also be considered including: commercial importance, world economy, trade deficits, and the like. The following example might shed some light.

In the beginning of this new 21st century, all the hundreds of IC companies worldwide could not break the 100 nm transistor size barrier. Of course, everybody **wanted** smaller, more miniaturized and higher-performing IC devices. But desire, want, or wish does not make inventions. Nobody anywhere seemed to make even 90 nm IC devices. In IC business, even the **seemingly negligible, insignificant 10% difference** in feature sizes or dimensions may means many years by thousands of highly skilled technicians working hard on difficult R&D worldwide, spending billions of dollars alone on new equipment, with **dozens or hundreds of newly patented technologies.** The fate of each hard-working technician, corporation, and country is at great stake, win or lose. Still, all believed that new materials must be found, new equipment developed, and new technologies perfected.

Luckily, shortly after Li's first atomic patent (No. 6,599,781) came out, Intel tried the first of several approaches in the patent by "having silicon sitting on top of intrinsic silicon" to totally eliminate the normally unavoidable, damaging thermal mismatch stresses between the different component materials. In a few weeks, the leakage current dropped by orders of magnitude. The Second worldwide leakage current problem suddenly disappeared. IC with 90 and 65 nm

through 5, 7, 8, and 10 through 19 under 35 USC 103 as anticipated by Peltzer."

In the same decision on page 6, lines 12-21, the Board says: "As for claims 2 through 5, 7, 8 and 10 through 19, Murphy (RE 2,653) clearly does **not disclose** a groove depth that varies along a major portion of the groove width, a requirement of all these claims. For the reasons we expressed before with respect to Peltzer, we cannot say that appellant and Murphy form their grooves in the **same manner**. Finally, the examiner had not presented any other reason why this feature would have been **obvious**, and we know of none. Therefore, the rejection of claims 2 through 5, 7, 8, and 10 through 19 under 35 USC 103 as obvious in view of Murphy is reversed."

That is, both Peltzer and Murphy failed to teach, suggest, or even hint the Li's important groove rounding inventions. The reasons, the requirements, how to do it, what benefits, effect on device yield, cost and miniaturization, and the like, are not in the references.

For over 25 years after this decision, there were no more examiner's rejections of Li's groove having major-portion groove bottom of zero width, based on nothing but draftsman's accidental disclosure of seemingly rounded groove bottoms.

The importance of groove rounding to modern IC can be seen as follows. The Institute of Electrical and Electronics Engineers (IEEE) commemorated its 40th anniversary by asking 40 of the technology masterminds to vote on the most important technologies. The results are summarized in the November 2004 issue of the IEEE's Spectrum magazine at the tops of pages 38 and 39. "Take away the semiconductor, and all of **electronics** -- all of it! -- **collapses**, along with all of the world's economies." That's how Nick Holonyak, Jr., University of Illinois professor, IEEE medal of Honor winner, and

inventor of the red light-emitting diode, views the incalculable contribution that the IC has made to society over the last four decades. According to Craig R. Barrett, CEO of Intel Corporation, the world's largest semiconductor manufacturer "the most important technology of the last 40 years" is the commercialization of the transistor. Without the invention of the integrated circuit (IC), the personal computer would have been the size of the **Pentagon**, and the cell phone he size of the **Washington Monument.**"

The **inert** oxide isolating grooves in the prior-art devices, such as those of Peltzer (at. No. 3,648,125) and Murphy (Pat. No. 3,649,386), had central flat bottoms wastefully occupying major portions of the chip real-estate. This waste of chip real-estate resulted in only a **minor** portion of the chip used for the active transistors or diodes. See, Peltzer's '125, at col. 3, lines 22-25. These prior art devices made device miniaturization and modern microelectronics impossible.

All the claims to the IC remaining in the case are limited to **commercially mass-produced** devices, **with profit**, and exactly controlled to achieve submicron accuracy in depth, width, lateral locations, and accuracies. But there were no commercial equipment available anywhere in the world to make the IC device features smaller than the specified, i.e., submicrons. See. Attached reference chart Fig. 1 and Li's '081, col. 11, lines 31-32.

One example of the superior quality of the new IC commercially mass-produced was evidenced by the following: In late 1970's, Stanford University had a research project to study the human brains. They searched worldwide, because they needed diodes with the lowest leakage currents so the brains would have no residual memories. They picked General Instrument Corporation, where Li was in charge of material and techniques R&D.

The examiner was correct in stating that each of the '081 claimed IC is of the same **general** design and structure as those in the '800 patent. That, of course, is evident in the decision of the Larkins-initiated Interference #98,426 which decided that Li was the senior most inventor of the MOS or CMOS process, months or even years ahead of Fairchild's Peltzer Isoplanar device, Philips' Kooi CMOS, and IBM's Magdos' oxide recessed devices.

But the final product of said claim is **not** the same as **or obvious** over the prior. There simply were **no technologies and equipment** in 1973 to produce a single integrated IC device, according to Li's '800 patent. Hence, In *re Thorpe, 777 F3d 695, 698, 227 USPQ 964 (Fed. Cir. 1985)* simply does **not** apply.

The '102 application (Pat. No. 4,946,800) and this '081 application are totally different in Integrated circuit technologies. Hundreds or thousands valid patents separate these two applications. Even though they both are on Li's basic CMOS device and process designs, but the equipment, procedures, characteristics, are patentably different.

Notice in particular the '081 invention claims only "commercially mass-produced integrated circuits that must have high yield and low cost to withstand the fierce worldwide competition. The '081 devices are thousands or millions of times more dense on each chip. With a same production **component** yield of, e.g., 95 or even 99%, the final product chip yield can be commercially reasonable and profitable with the '800 process, but always zero or near zero with the '081 commercial mass-production process. This is because of the much larger number (thousands or millions) of IC components on each chip. Yet commercial mass-production of the '081 device was **non-existent** in 1973. There simply were no equipment and technologies to make the

'081 near micron size IC components. Hence, whatever the '800 says, the patent is not relevant to this '081.

The amended claim 1 further includes the following new limitation supported by the original specification in Table 4 on page 14, line 26, but non-existent in '800: "the lower curved bottom of said solid state material region having a radius of curvature of less than 0.1 microns and located at a depth of less than h = 0.1 microns to have an equivalent bevel angle of less than 0.810 radians." Also, Claim 1 is restricted to atomic IC, non-thought by practically all in 1973.

Claim Rejections - 35 U.S.C. 103

Claims 52-54, 56 and 65-71 are rejected under 35 U.S.C. 103(a) as being anticipated by Li (U.S. Patent #4946800).

All the arguments and new evidences given above apply equally well for these last claim rejections under 35 U.S.C. 103.

none. The '081 devices were, in 2004, **orders of magnitude** smaller in feature sizes, critical gate layer thicknesses, and packing densities than what were possible or patented, by Li or anybody else.

It is well known that small differences in sizes, dimensions, and accuracy are not patentable. Do the **orders of magnitude** size differences between the '800 and '081 inventions patentable? These is no absolute numbers to distinguish between patentability and non-patentability. Other factors must also be considered including: commercial importance, world economy, trade deficits, and the like. The following example might shed some light.

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Luckily, shortly after Li's first atomic patent (No. 6,599,781) came out, Intel tried the first of several approaches in the patent by "having silicon sitting on top of intrinsic silicon" to totally eliminate the normally unavoidable, damaging thermal mismatch stresses between the different component materials. In a few weeks, the leakage current dropped by orders of magnitude. The Second worldwide leakage current problem suddenly disappeared. IC with 90 and 65 nm

transistors also became possible, rapidly going down to even 35 or 20 nm, and by several companies.

Hence, the '800 patent is totally irrelevant and useless to commercially mass-produce the '081 IC devices. More details and discussions will be given immediately.

For another reason the '800 invention does not work for the '800 devices, one needs to take a side step. "Major-portion groove bottom rounding" is a key feature of Li's unique oxide-isolation grooves leading to high device yield, low cost, extreme miniaturization, passivated PN junctions, low leakage currents, high breakdown voltages, and many other benefits. The current '081 invention still relies heavily on this rounding technology.

Many prior examiners have repeatedly rejected this critical rounding feature under USC section 103. These rejections were all overcome or reversed. The 05/838,758 (patent 4,916,513) Appeals Board on June 17, 1981 on page 5, line 4-21 decisively stated that: "claims 2 through 5, 7, 8 and10 through 19 all require that the depth of the groove vary along a major portion (more than half) of the groove width. **Peltzer** (Pat. No 3,648,125) does **not explicitly** disclose this feature. Nor is it apparent from the drawings that the curved portions at the bottom of the groove extend over more than half of the width of the groove. The examiner says that the appellant and Peltzer form their grooves in **exactly the same manner**; therefore, they must be **identical**. While Peltzer says that the grooves are etched in the epitaxial layer and then oxidized to form oxide isolation regions, no mention is made of the **cross-sectional shape** of the grooves. The appellant, on the other hand, is **very concerned** about the **cross-sectional shape** of the groove. Therefore, we cannot say that the grooves of the appellant and Peltzer are formed in exactly the same manner. Therefore, we will not sustain the rejection of claims 2

Exhibit A: Li's Atomic IC

Family Tree of Li's Atomic IC Inventions

Pat. 6,599,781, Ser. No. 09/670,571, filed 09/27/2000
on "Solid state Device"

Pat. 6,784,515, Ser. No. 09/670,874, filed 09/27/2000
On Semiconductor Integrated Circuit Device

Pat. 7,118,942, Ser. No. 10/630,115, filed 07/29,2003
On "Method of Making atomic Integrated Circuit Device"

Ser. No. 10/759,081, filed 01/20/2004
On "integrated Circuit Device"

Exhibit B: Moore's Law

Electronic Engineering Times, Feb 16, 1998 p.1

Solid State

Semiconductor scaling close to its limits